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Box Patent Application
Commissioner for Patents
Washington, DC 20231

Presented for filing is a new original patent application of:

Applicant: KEIJI NEGI

Title: PATTERN SYNCHRONOUS CIRCUIT

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Enclosed are the following papers, including those required to receive a filing date under 37 CFR §1.53(b):

	Pages
Specification	23
Claims	3
Abstract	1
Declaration	3
Drawing(s)	6

Enclosures:

- Assignment cover sheet and an assignment, 4 pages, and a separate $40 fee.
- Preliminary amendment, 4 pages.
- Certified copy of priority document no. 11-337871.
- Postcard.

Under 35 USC 119, this application claims the benefit of a foreign priority application filed in Japan, serial number 11-337871, filed November 29, 1999.

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Basic filing fee	$710
Total claims in excess of 20 times $18	$0
Independent claims in excess of 3 times $80	$0
Fee for multiple dependent claims	$0
Total filing fee:	$710

A check for the total filing fee is enclosed. Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

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Respectfully submitted,

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Enclosures
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Keiji Negi	Art Unit	: Unknown
Serial No.	: Not yet assigned	Examiner	: Unknown
Filed	: November 27, 2000		
Title	: PATTERN SYNCHRONOUS CIRCUIT		

Commissioner for Patents
Washington, D.C. 20231

Box Patent Application

PRELIMINARY AMENDMENT

Prior to examination, please amend the application as follows:

In the Claims: A marked-up version of the amended claims is provided on separate attached sheets.

Please amend the claims as follows:

4. (Amended) The pattern synchronous circuit as defined in claim 2 wherein said shift means shifts bits without sorting a list of the parallel signals according to the frame position information.

5. (Amended) The pattern synchronous circuit as defined in claim 2 wherein said sort means sorts a list of bits in the same clock of the parallel signals according to the frame position information.

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6. (Amended) The pattern synchronous circuit as defined in claim 1 wherein the low order bit of the frame position information outputted by said frame detection means has the number of bits sufficient to indicate values of the number m of shift means constructing said second sort means.

Add the following new claims:

7. (New) The pattern synchronous circuit as defined in claim 3 wherein said shift means shifts bits without sorting a list of the parallel signals according to the frame position information.

8. (New) The pattern synchronous circuit as defined in claim 3 wherein said sort means sorts a list of bits in the same clock of the parallel signals according to the frame position information.

9. (New) The pattern synchronous circuit as defined in claim 2, wherein the low order bit of the frame position information outputted by said frame detection means has the number of bits sufficient to indicate values of the number m of shift means constructing said second sort means.

10. (New) The pattern synchronous circuit as defined in claim 3, wherein the low order bit of the frame position information outputted by said frame detection means has the number of bits sufficient to indicate values of the number m of shift means constructing said second sort means.

REMARKS

Claims 4, 5 and 6 have been amended to remove multiple dependencies.

Claims 1-10 are pending.

Applicant submits that all of the claims are in condition for examination, which action is requested. Please apply any other charges or credits to Deposit Account

No. 06-1050.

Respectfully submitted,

Date: 11-27-2000

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MARKED-UP VERSION OF THE AMENDED CLAIMS

4. (Amended) The pattern synchronous circuit as defined in claim 2 [or 3,] wherein

said shift means shifts bits without sorting a list of the parallel signals according to the frame position information.

5. (Amended) The pattern synchronous circuit as defined in claim 2 [or 3,] wherein

said sort means sorts a list of bits in the same clock of the parallel signals according to the frame position information.

6. (Amended) The pattern synchronous circuit as [in any one of claims 1 to 3] defined in claim 1, wherein

the low order bit of the frame position information outputted by said frame detection means has the number of bits sufficient to indicate values of the number m of shift means constructing said second sort means.

30033597.doc

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: PATTERN SYNCHRONOUS CIRCUIT

APPLICANT: KEIJI NEGI

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PATTERN SYNCHRONOUS CIRCUIT

BACKGROUND OF THE INVENTION

This invention relates to a pattern synchronous circuit for sorting a parallel signal so that a signal evaluation can be made to a signal after making a serial-parallel conversion of an inputted evaluation pattern in a pattern evaluation apparatus for evaluating a frame signal.

A frame signal having a frame identification pattern is used in a transmission device test.

In this kind of test, a pattern based on actual transmission standards is outputted from a pulse pattern generator and is inputted to an evaluation device unit and the output is observed by a pattern evaluation apparatus or an oscilloscope.

The pattern evaluation apparatus normally makes a serial-parallel conversion to a received signal and reduces the signal to a signal speed easy to process and conducts the evaluation. However, timing of inputting the received signal is not determined, so that a leading position of a frame is not determined in a signal after the serial-parallel conversion. As a result of that, it must be constructed so that subsequent evaluations can be made by detecting the frame identification pattern and sorting a parallel signal.

Fig. 11 shows a configuration of a pattern evaluation

apparatus after the serial-parallel conversion. In Fig. 11, numeral 1 is a parallel signal input terminal to which a signal changing a received signal into n parallel signals is inputted, and numeral 2 is a clock input terminal, and numeral 31 is a branch circuit, and numeral 32 is a frame detection circuit, and numeral 33 is a shift circuit, and numeral 34 is a measurement circuit, and numeral 35 is a frame position signal, and numeral 300 is a pattern synchronous circuit.

The signal changing the received signal into the n parallel signals is inputted to the frame detection circuit 32 and the shift circuit 33 through the branch circuit 31.

A clock signal for processing a parallel signal is inputted to the clock input terminal 2. In the frame detection circuit 32, a parallel input signal is monitored and a frame identification pattern is detected and a signal indicating its place is outputted to the frame position signal 35. The shift circuit 33 is a sort circuit for sorting the parallel input signal and in the shift circuit 33, the parallel input signal is sorted by the frame position signal 35 and in the measurement circuit 34, an output is produced so that it becomes a measurable state, namely the lead of a frame becomes a leading position of the parallel signal.

In this case, the shift circuit 33 can implement a pattern synchronous operation by performing processing as described in a truth table shown in Fig. 12, for example, when the number

n of parallel signals is 16. The truth table shown in Fig. 12 indicates that SEL corresponds to a frame position signal and a signal is selected from the parallel signals of 16 bits as shown in output by SEL input and is outputted. Also, the places described as A(+1), B(+1), C(+1), ··· indicate signals after one clock of inputs A, B, C, ···.

Here, when the shift circuit 33 of Fig. 11 produces an increase in circuit scale, particularly an increase in the number n of signals, integration into one integrated circuit becomes difficult. Thus, the shift circuit 33 is implemented by a plurality of integrated circuits.

Next, a pattern synchronous circuit according to a conventional art will be described using Fig. 7. In Fig. 7, numeral 1 is a parallel signal input terminal, and numeral 2 is a clock input terminal, and numeral 3 is a parallel signal output terminal, and numeral 21 is a branch circuit, and numeral 22 is a frame detection circuit, and numeral 23 is a shift part, and numerals 24a to 24d are shift circuits A to D constructing the shift part 23, and numeral 25 is a frame position signal. The shift part 23 comprises a plurality of the shift circuits 24a to 24d. As a result of that, the shift circuit per circuit performs sorting of the number n of parallel signals and data processing of the number divided by the number m of integrated circuits.

A signal inputted to the parallel signal input terminal

1 is branched to the frame detection circuit 22 and all the shift circuits 24a to 24d through the branch circuit 21. The frame detection circuit 22 detects a frame identification pattern in the parallel signals and outputs a signal to the frame position signal 25. The frame position signal 25 is connected to all the shift circuits 24a to 24d, and the shift circuits 24a to 24d sort the parallel signals by the frame position signal 25.

As examples, Figs. 8 and 9 indicate truth tables showing operations of the shift circuit A and the shift circuit B where the number n of parallel signals is 16 bits and four shift circuits are used.

When the frame position signal is 0, the shift circuit A outputs signals A, B, C, D inputted to D0 to D3. At that time, the shift circuit B outputs signals E, F, G, H inputted to D4 to D7 since the shift circuit B outputs signals subsequent to the signals outputted by the shift circuit 24a. Also, when the frame position signal is 1, the shift circuit 24a outputs signals B, C, D, E inputted to D1 to D4, and the shift circuit 24b outputs signals F, G, H, I which are signals subsequent to the signals outputted by the shift circuit 24a. Truth tables of operations of the shift circuit 24c and the shift circuit 24d are omitted, but the truth tables can be derived in a manner similar to truth values of Figs. 8 and 9.

Operations of a pattern synchronous circuit 200 of Fig.

7 will be described concretely using Figs. 10A and 10B.

It is assumed that the number of parallel signal inputs is 16 bits and for the purpose of illustration, parallel signals of 16 bits are described as a, b, c, ···, o, p and the leading of a frame begins with a. Expressions such as p(-1) indicate a bit earlier than p by one clock.

Figs. 10A and 10B show an example in which a frame of an input signal begins with BIT 7 of the parallel signal input terminal. The frame detection circuit 22 outputs a value 7 to the frame position signal 25 when detecting the frame in beginning with BIT 7. Then, the shift circuit 24a selects BITs 7 to 10 from the parallel signals of 16 bits, and also the shift circuit 24b selects BITs 11 to 13 and outputs them. Similarly, the shift circuits 24c and 24d select respectively corresponding 4 bits from input signals and thereby, an output signal in which the leading of the frame begins with BIT 0 of the parallel signals as a whole can be obtained.

Here, all the information of the inputted parallel signals needs to be inputted to all the shift circuits 24a to 24d in order to cope with a start position of the frame in all the states. For that purpose, all the bits of the input signals are branched to all the shift circuits 24a to 24d by the branch circuit. Then, all the shift circuits 24a to 24d require the number of input I/Os corresponding to the number n of parallel bits of the input signals.

As described above, in the pattern synchronous circuit according to the conventional art, all the bits of the parallel signals inputted to the parallel signal input terminal 1 are branched by the branch circuit 21 and are inputted to all the shift circuits 24a to 24d constructing the shift part 23. Then, the respective shift circuits 24a to 24d select only the number of signals obtained by dividing the number n of parallel signals of the output signals by the number of sort integrated circuits from the input signals and output it on the basis of the frame position signal 25 outputted by the frame detection circuit 22. An output signal in which the frame begins with BIT 0 of the parallel signals can be obtained by merging outputs of all the shift circuits 24a to 24d.

However, in the conventional pattern synchronous circuit described above, an input signal is branched to all the shift circuits, so that the number of wirings increases in proportion to the number n of parallel signals and the number m of shift circuits. Also, since all the bits of a parallel signal input are inputted to the shift circuits, the number of I/Os of the shift circuits becomes large with an increase in the number n of parallel signals and thus a large package is required. As a result of that, miniaturization of the pattern synchronous circuit is difficult.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a pattern synchronous circuit capable of achieving miniaturization by reducing the number of wirings between elements or the number of I/Os of the elements particularly when the number n of parallel input signals becomes large and a sort circuit is formed of a plurality of integrated circuits.

The invention can achieve the object by performing a configuration of a pattern synchronous circuit as follows.

No. 1. A pattern synchronous circuit comprises branch means for branching parallel signals of n bits inputted from a parallel signal input terminal into two portions, frame detection means for using one portion of the parallel signals branched by the branch means as input and detecting a frame identification pattern in the parallel signals to output the position information, first sort means for using the other portion of the parallel signals branched by the branch means as input and sorting the parallel signals according to a low order bit of the frame position information outputted by the frame detection means, and second sort means for further using outputs of the first sort means as input and again sorting the parallel signals according to all the bits of the frame position information outputted by the frame detection means.

No. 2. The first sort means comprises one shift means for using (n/l)-th bit from the first bit of the parallel

signals as input and performing shift operations according to a low order bit of the frame position information outputted by the frame detection means, and (l-1) sort means for respectively using (n/l) bits in the continuous parallel signals as input and performing sort operations according to a low order bit of the frame position information outputted by the frame detection means.

No. 3. The second sort means comprises delay means for using data obtained by sampling the first sort means every m bits as input and delaying signals, (m-1) sort means for respectively using data obtained by sampling the mutually different first sort means every m bits as input and performing sort operations according to a low order bit of the frame position information outputted by the frame detection means, and m shift means for respectively using outputs of the delay means and the sort means as input and performing shift operations according to a high order bit of the frame position information outputted by the frame detection means.

No. 4. The shift means of Nos. 2-3 shifts bits without sorting a list of the parallel signals according to the frame position information.

No. 5. The sort means of Nos. 2-3 sorts a list of bits in the same clock of the parallel signals according to the frame position information.

No. 6. The low order bit of the frame position information

outputted by the frame detection means has the number of bits sufficient to indicate values of the number m of shift means constructing the second sort means.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of one embodiment of a pattern synchronous circuit according to the invention;

Fig. 2 is a truth table showing operation examples of a shift circuit A and sort circuits A to D of the embodiment;

Fig. 3 is a truth table showing operation examples of shift circuits B to D of the embodiment;

Fig. 4 is a truth table showing operation examples in an enable state of one-bit shift circuits A to C of the embodiment;

Figs. 5A and 5B are operational diagrams of a shift circuit 6 of the embodiment;

Figs. 6A to 6C are operational diagrams of a sort circuit 7 of the embodiment;

Fig. 7 is a block diagram of a conventional example;

Fig. 8 is a truth table showing operation examples of a sort circuit A of the conventional example;

Fig. 9 is a truth table showing operation examples of a sort circuit B of the conventional example;

Figs. 10A and 10B are operational diagrams of the conventional example;

Fig. 11 is a block diagram illustrating a circuit configuration of a pattern synchronous circuit; and

Fig. 12 is a truth table showing operation examples of a sort circuit in the block diagram of Figs. 10A and 10B.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Next, the invention will be described with reference to the accompanying drawings. Fig. 1 is a block diagram showing an embodiment of the invention. In Fig. 1, numeral 1 is a parallel signal input terminal, and numeral 2 is a clock input terminal, and numeral 3 is a parallel signal output terminal, and numeral 4 is a branch circuit, and numeral 5 is a frame detection circuit, and numeral 6 is a first sort part, and numeral 7 is a second sort part, and numeral 8 is a shift circuit of the first sort part, and numerals 9a to 9c are sort circuits of the first sort part, and numeral 10 is a delay circuit, and numerals 11a to 11c are sort circuits of the second sort part, and numerals 12a to 12d are shift circuits of the second sort part, and numeral 13 is a low order bit of a frame position signal, and numeral 14 is a high order bit of the frame position signal.

Then, the block diagram of Fig. 1 will be described shortly. In a manner similar to a conventional example, a parallel signal of n bits in which a serial-parallel conversion of a signal to be measured is made is inputted to the parallel

signal input terminal 1. Also, a pattern synchronous circuit 100 operates on a clock inputted to the clock input terminal 2, and the processed parallel signal of n bits is outputted to the parallel signal output terminal 3.

Data inputted to the parallel signal output terminal 1 is distributed to the frame detection circuit 5 and the first sort part 6 through the branch circuit 4. In a manner similar to the conventional example, the frame detection circuit 5 monitors a frame identification pattern from the inputted signal and detects which bit of a parallel signal the frame identification pattern starts with and outputs its result to a low order bit 13 of the frame position signal and a high order bit 14 of the frame position signal.

In the first sort part 6, the low order bit 13 of the frame position signal is used as input and the other processing of a signal branched by the branch circuit 4 is performed. The first sort part 6 is constructed of one shift circuit 8 and (l-1) sort circuits 9a to 9c where the number of components operating in parallel is l. In the block diagram of Fig. 1, an example of setting l to 4 is described, but a value of l is arbitrary and the similar effect can be obtained for other values. In the shift circuit 8 and the sort circuits 9a to 9c, respectively, the number of signals obtained by dividing the number n of parallel signals by the number m of components operating in parallel is used as input and processing is

performed. In respective components, BITs 0 to (n/l-1) of the parallel signals are inputted to the shift circuit 8 of the first sort part and BITs (n/l) to (2n/l-1) are inputted to the sort circuit 9a and BITs (2n/l) to (3n/l-1) are inputted to the sort circuit 9b and BITs (3n/l) to (4n/l-1) are inputted to the sort circuit 9c in bit sequence in serial of the parallel signals.

The shift circuit 8 of the first sort part performs operations as shown in Fig. 2, for example, when the number of inputs of the shift circuit 8 is four. The shift circuit 8 performs processing of bit-shifting an input signal in a parallel direction according to a state of SEL input, namely the low order bit 13 of the frame position signal. For example, when SEL is 0, data is outputted without any processing, and when SEL is 1, a signal inputted to D1 is outputted to Q0 and a signal inputted to D2 is outputted to Q1 and a signal inputted to D3 is outputted to Q2 and a signal in which a signal inputted to D0 is delayed by one clock is outputted to Q3. When SEL is 2 or 3, data in which subsequently similar shift is performed is outputted.

Also, the sort circuits 9a to 9c of the first sort part performs operations as shown in Fig. 3, for example, when the number of inputs of the sort circuits 9a to 9c is four. The sort circuits 9a to 9c perform processing of sorting within bits of the same clock of an input signal according to a state

of SEL input, namely the low order bit 13 of the frame position signal. For example, when SEL is 0, data is outputted without any processing, and when SEL is 1, a signal inputted to D1 is outputted to Q0 and a signal inputted to D2 is outputted to Q1 and a signal inputted to D3 is outputted to Q2 and a signal inputted to D0 is outputted to Q3. When SEL is 2 or 3, data in which subsequently similar sort is performed is outputted.

As described above, sort processing of a first step is first performed by the shift circuit 8 of the first sort part and the sort circuits 9a to 9c of the first sort part according to the low order bit 13 of the frame position signal. The parallel signals of n bits outputted by the first sort part 6 are inputted to the second sort part 7.

The second sort part 7 is constructed of one delay circuit 10, (m-1) sort circuits 11a to 11c for performing processing by the low order bit 13 of the frame position signal and m shift circuits 12a to 12d for performing processing by the high order bit 14 of the frame position signal. In the block diagram of Fig. 1, an example of setting m to 4 is described, but a value of m is arbitrary in a manner similar to the value of 1 and other values may be used.

In signals inputted to the second sort part 7, the signals sampled every m bits as BIT 0, BIT m, BIT 2m, ···, BIT (n-1)·m are inputted to the delay circuit 10. Also, signals in which the signals inputted to the delay circuit 10 are shifted by

one bit as BIT 1, BIT (m+1), BIT (2m+1), ···, BIT ((n-1)·m+1) are inputted to the next sort circuit 11a. Similarly, signals in which the signals inputted to the sort circuit 11a are shifted by one bit are inputted to the sort circuit 11b, and signals in which the signals inputted to the sort circuit 11b are further shifted by one bit are inputted to the sort circuit 11c.

Outputs of the delay circuit 10 and the sort circuits 11a to 11c are inputted to the shift circuits 12a to 12d of the same line. The shift circuits 12a to 12d perform processing by the high order bit 14 of the frame position signal. Signals processed by the shift circuits 12a to 12d are outputted to the parallel signal output terminal 3. At this time, the respective shift circuits 12a to 12d output the signals sampled every m bits in a manner similar to the input.

Operations of the second sort part 7 will be described shortly. The sort circuits 11a to 11c monitor the low order bit 13 of the frame position signal and perform an operation shown in a truth table of Fig. 4 when enable conditions are satisfied. The operation shown in the truth table of Fig. 4 means the same operation as the case that SEL is 1 in the truth table of the sort circuits of Fig. 3. Here, the enable conditions mean the time when the low order bit 13 of the frame position signal becomes (m-1) in the sort circuit 11a for monitoring a line of BIT 1 and also, the time when the low order

bit 13 of the frame position signal becomes (m-2) or more in the sort circuit 11b for monitoring a line of BIT 2 and the time when the low order bit 13 of the frame position signal becomes (m-3) or more in the sort circuit 11c for monitoring a line of BIT 3. The respective sort circuits 11a to 11c of the second sort part perform the operations of Fig. 4 when the enable conditions are satisfied and produce outputs without any processing as it is when the enable conditions are not satisfied.

Generally speaking of this operation, first, a value of a frame detection signal is divided by the number m of parallel processing components of the second sort part. Next, when its remainder is 0 or larger, the delay circuit 10 and the sort circuits 11a to 11c produce outputs without any processing, and when the remainder is 1, the sort circuit for processing BIT (m-1) becomes an enable state. Also, when the remainder is 2, the sort circuit for processing BIT (m-1) and BIT (m-2) becomes an enable state. When the remainder is 2 or larger, the sort circuit for processing subsequent BIT (m-3), ··· becomes an enable state. Here, the low order bit 13 of the frame position signal means the remainder obtained by dividing the value of the frame detection signal by the number m of parallel processing components of the second sort part, and the high order bit 14 of the frame position signal means the quotient obtained by dividing the value of the frame detection

signal by the number m of parallel processing components of the second sort part.

In the delay circuit 10, delays are caused by the time necessary for processing of the sort circuits 11a to 11c of the second sort part and a signal is outputted. Then, outputs of the delay circuit 10 and the sort circuits 11a to 11c are inputted to the shift circuits 12a to 12d of the same line, and the shift circuits 12a to 12d perform operations shown in the truth table of Fig. 2 based on the high order bit 14 of the frame position signal. The shift circuits 12a to 12d perform processing of bit-shifting an input signal in a parallel direction according to a state of SEL input, namely the high order bit 14 of the frame position signal. For example, when SEL is 0, data is outputted without any processing, and when SEL is 1, a signal inputted to D1 is outputted to Q0 and a signal inputted to D2 is outputted to Q1 and a signal inputted to D3 is outputted to Q2 and a signal in which a signal inputted to D0 is delayed by one clock is outputted to Q3. When SEL is 2 or 3, data in which subsequently similar shift is performed is outputted. Then, outputs of the shift circuits 12a to 12d are connected to the parallel signal output terminal 3, and a signal in which a frame identification pattern is shifted to BIT 0 is outputted.

Operations of a pattern synchronous circuit 100 of Fig. 1 will be described concretely using Figs. 5A, 5B, and 6A to

6C. In a manner similar to the conventional example of Figs. 10A and 10B, Figs. 5A and 5B show an example in which the number n of parallel signals is 16 bits and the number l of parallel processing components of the first sort part is four and the number m of parallel processing components of the second sort part is four and a frame of an input signal begins with BIT 7 of the parallel signal input terminal.

The frame detection circuit 5 detects that the frame begins with BIT 7. At this time, a value 3 which is the remainder obtained by dividing a value 7 of the frame position signal by the number m (where m=4) of parallel processing components of the second sort part is outputted to the low order bit 13 of the frame position signal. Also, a value 1 which is the quotient obtained by dividing a value 7 of the frame position signal by the number m (where m=4) of parallel processing components of the second sort part is outputted to the high order bit 14 of the frame position signal.

First, since the low order bit of the frame position signal is 3, an output of each the shift circuit 8 and the sort circuits 9a to 9c can be obtained as shown in Figs. 5A and 5B. That is, in the shift circuit 8 inputted as j(-1), k(-1), l(-1), m(-1), results of m(-1), j, k, l can be obtained from the operations of the truth table of Fig. 2, and in the sort circuit 11a inputted as n(-1), o(-1), p(-1), a, results of a, n(-1), o(-1), p(-1) can be obtained from the operations of the truth

table of Fig. 3. As a result, data strings of m(-1), j, k, l, a, n(-1), o(-1), p(-1), ···, g, h are outputted as data of point A of Fig. 1.

Next, operations of the second sort part will be described by way of Figs. 6A to 6C. In the second sort part, a list of signals is shown by sorting the list every processing line since the processing line is processed in a sampled signal line. In the delay circuit 10, BITs 0, 4, 8, 12 of a line of BIT 0 of parallel signals are inputted, and delays are caused by the time necessary for processing of the sort circuits 11a to 11c of the second sort part and an output is produced. In Figs. 6A to 6C, m(-1), a, e, i are outputted as it is since BITs 0, 4, 8, 12 are m(-1), a, e, i.

The sort circuits 11a to 11c of the second sort part perform operations shown in the truth table of Fig. 4 with respect to all the sort circuits since the low order bit of the frame position signal is 3. Since j, n(-1), b, f are inputted to the sort circuit 11a of the second sort part for processing a line of BIT 1 of parallel signals, n(-1), b, f, j are outputted. For the sort circuits 11b and 11c of the second sort part for processing lines of BIT 2 and BIT 3 of parallel signals, processing is performed and generates state signals at point B as a whole.

Thereafter, an output of the delay circuit 10 is inputted to the shift circuit 12a and outputs of the sort circuits 11a

to 11c are inputted to the shift circuits 12b to 12d. In the respective circuits, the operations of the time when SEL of Fig. 2 is 1 are performed since the high order bit of the frame position signal is 1. As a result of that, the shift circuit 12a outputs data strings of a, e, i, m, and the shift circuit 12b outputs data strings of b, f, j, n, and the shift circuit 12c outputs data strings of c, g, k, o, and the shift circuit 12d outputs data strings of d, h, l, p. These are the data strings in which a begins with BIT 0. That is, there are the data strings in which a frame begins with BIT 0.

Frame synchronization is provided by the operations described above. In the examples of Figs. 5 and 6, a pattern in which a frame starts with BIT 7 is used, but even when a frame pattern begins with other lines, input data can be shifted to data strings in which the frame begins with BIT 0 of parallel signals by the operations described above.

In the pattern synchronous circuit of the invention, input data is branched at the branch circuit and one of the branched data is data for frame detection and the other of the branched data is data for sort. Then, frame synchronous processing is performed with respect to the signal for sort at two steps of the first sort part 6 and the second sort part 7. The number of I/Os of respective components of the first sort part 6 and the second sort part 7 can be implemented with the number obtained by dividing the number n of bits of parallel

signals by the number l, m of components operating in parallel. Also, components (for example, the delay circuit 10 and the shift circuit 12a) for processing the same line of the second sort part 7 can be integrated into the same package and in this case, components of the second sort part 7 can also be implemented by m integrated circuits.

Incidentally, the pattern synchronous circuit of the invention is not limited to a circuit configuration of the pattern synchronous circuit shown in the embodiment described above, but other circuit configurations may be used of course as long as there is a circuit configuration capable of obtaining the similar effects.

In the invention according to aspect 1, signals inputted from a parallel signal input terminal are branched into two portions by branch means and are outputted, and one portion becomes an output signal for detection of a frame identification pattern and the other portion becomes an output signal for measurement after sorting.

Therefore, the number of branches of the input signals can be constructed at a minimum, so that the number of wirings between elements can be reduced and an effect of reducing a packaging area of a pattern synchronous circuit can be obtained.

In the invention according to aspect 2, first sort means is constructed of l elements having inputs and outputs of data

of n/l bits, and performs shift operations and sort operations, respectively.

Therefore, the number of I/Os of the respective elements can be decreased, so that a smaller package can be used and an effect of reducing a packaging area of a pattern synchronous circuit can be obtained.

In the invention according to aspect 3, second sort means is constructed of m×2 elements having inputs and outputs of data of n/m bits, and performs shift operations and sort operations, respectively.

Therefore, the number of I/Os of the respective elements can be decreased, so that a smaller package can be used and a packaging area of a pattern synchronous circuit can be reduced. Also, a set of the elements for processing the same line of parallel signals can further be integrated into one package and in such a case, an effect of further reducing the packaging area of the pattern synchronous circuit can be obtained.

In the invention according to aspect 4, it is indicated that shift operations are operations of shifting data in a parallel direction without changing a list of parallel signals.

Therefore, the shift operations can be implemented in a simple circuit configuration, so that integration into one package can be made and an effect of reducing a packaging area of a pattern synchronous circuit can be obtained.

In the invention according to aspect 5, it is indicated

that sort operations are operations of sorting bits of the same clock of parallel signals.

Therefore, the sort operations can be implemented in a simple circuit configuration, so that integration into one package can be made and an effect of reducing a packaging area of a pattern synchronous circuit can be obtained.

In the invention according to aspect 6, it is indicated that a low order bit of frame position information can comprise the number of bits sufficient to indicate values of the number m of shift means constructing the second sort means.

Therefore, by dividing sort means into the first sort means and the second sort means, the frame position information can be constructed at the minimum number of branches and thereby, and an effect of reducing a packaging area of a pattern synchronous circuit without an increase in the number of wirings can be obtained.

As described in detail above, a pattern synchronous circuit according to the invention can reduce the number of signals branched by a branch circuit. Therefore, in the pattern synchronous circuit according to the invention, the number of wirings does not increase in proportion to the number m, l of components operating in parallel.

Also, the number of I/Os of signal inputs of shift circuits and sort circuits constructing first and second sort parts is obtained by dividing the number n of bits of parallel

signals by the number m or l of components operating in parallel.

Therefore, in the shift circuits and the sort circuits constructing the first and second sort parts, even in case that the number n of parallel signals increases, the number of I/Os of the shift circuits does not increase and a small package can be constructed. As a result of that, the pattern synchronous circuit can be miniaturized.

As described above, the invention can achieve miniaturization by reducing the number of wirings between elements or the number of I/Os of the elements particularly when the number n of parallel input signals becomes large and a sort circuit is formed of a plurality of integrated circuits.

WHAT IS CLAIMED IS:

1. A pattern synchronous circuit comprising:

branch means for branching parallel signals of n bits inputted from a parallel signal input terminal into two portions,

frame detection means for using one portion of the parallel signals branched by said branch means as input and detecting a frame identification pattern in the parallel signals to output the position information,

first sort means for using the other portion of the parallel signals branched by said branch means as input and sorting the parallel signals according to a low order bit of the frame position information outputted by said frame detection means, and

second sort means for further using outputs of said first sort means as input and again sorting the parallel signals according to all the bits of the frame position information outputted by said frame detection means.

2. The pattern synchronous circuit as defined in claim 1, wherein

said first sort means comprises:

one shift means for using (n/1)-th bit from the first bit of the parallel signals as input and performing shift operations according to a low order bit of the frame position

information outputted by said frame detection means, and

(l-1) sort means for respectively using (n/l) bits in the continuous parallel signals as input and performing sort operations according to a low order bit of the frame position information outputted by said frame detection means.

3. The pattern synchronous circuit as defined in claim 1, wherein

said second sort means comprises:

delay means for using data obtained by sampling said first sort means every m bits as input and delaying signals,

(m-1) sort means for respectively using data obtained by sampling said mutually different first sort means every m bits as input and performing sort operations according to a low order bit of the frame position information outputted by said frame detection means, and

m shift means for respectively using outputs of said delay means and said sort means as input and performing shift operations according to a high order bit of the frame position information outputted by said frame detection means.

4. The pattern synchronous circuit as defined in claim 2 or 3, wherein

said shift means shifts bits without sorting a list of the parallel signals according to the frame position information.

5. The pattern synchronous circuit as defined in claim 2 or 3, wherein

said sort means sorts a list of bits in the same clock of the parallel signals according to the frame position information.

6. The pattern synchronous circuit as in any one of claims 1 to 3, wherein

the low order bit of the frame position information outputted by said frame detection means has the number of bits sufficient to indicate values of the number m of shift means constructing said second sort means.

ABSTRACT OF THE DISCLOSURE

Sort operations of an input signal are performed by providing a first sort part 6 comprising one shift circuit 8 and (l-1) sort circuits 9a to 9c, and a second sort part 7 comprising one delay circuit 10, (m-1) sort circuits 11a to 11c and m shift circuits 12a to 12d in a pattern synchronous circuit 100.

Declaration and Power of Attorney for Patent Application
特許出願宣言書及び委任状

Japanese Language Declaration
日本語宣言書

下記の氏名の発明者として、私は下記の通り宣言します：

As a below named inventor, I hereby declare that:

私の住所、郵送先、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の氏名が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PATTERN SYNCHRONOUS CIRCUIT

上記発明の明細書（下記の欄で×印がついていない場合は、本状に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ ___年___月___日に提出され、米国出願番号または特許協力条約国際出願番号を__________とし、（該当する場合）___年___月___日に訂正されました。

☐ was filed on ________________
as United States Application Number or
PCT International Application Number
____________ and was amended on
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私は、特許請求範囲を含む上記補正による補正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendement referred to above.

私は、連邦規則法典第３７編第１条５６項に規定されるとおり、特許性の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Declaration and Power of Attorney for Patent Application
特許出願宣言書及び委任状

私は、米国法典第３５編１１９条 (a) - (d) 項又は３６５条(b) 項に基づき下記の、米国以外の国の少なくとも一カ国を指定している同編３６５条 (a) 項に基づく特許協力条約国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願または特許協力条約国際出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority not claimed 優先権主張なし
P. HEI 11-337871	Japan	29/November/1999	☐
			☐

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基づいて下記の米国特許出願の権利、又は米国を指定している特許協力条約国際出願３６５条 (c) に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項で規定された態様で先行する米国特許出願または特許協力条約国際出願に開示されていない限り、連邦規則法典第３７編１条５６項で定義されたその先行米国出願書提出日以降で国内または特許協力条約国際提出日までの期間中に入手し得た、特許性に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, isofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の表明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Declaration and Power of Attorney for Patent Application
特許出願宣言書及び委任状

委任条：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する代理人として、下記の者を指名いたします。*(代理人の氏名及び登録番号を明記のこと)*

POWER OF ATTORNEY: as named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

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